IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 17463US02

In the Application of:	Theodore Trost et al.
U.S. Serial No.:	09/788,061
Filed:	February 16, 2001
For:	BLUETOOTH BASEBAND SOLUTION WITH REDUCED PROCESSOR REQUIREMENTS AND INTEGRATED HOST CONTROLLER
Examiner:	Eugene Yun
Group Art Unit:	2618
Confirmation No.:	5102
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/Michael T. Cruz/
Michael T. Cruz
Reg. No. 44,636

REVISED APPEAL BRIEF
IN RESPONSE TO
NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is a Revised Appeal Brief in response to the Notification of Non-Compliant Appeal Brief ("the Notification") mailed June 27, 2007. The deadline by which to file a Revised Appeal Brief is July 27, 2007.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 5300 California Avenue, Irvine, California 92617, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor.

RELATED APPEALS AND INTERFERENCES

There are currently no appeals or interferences pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-14 are pending and are being prosecuted in the present application. Claims 1-14 stand rejected. The rejection of claims 1-14 is being appealed.

STATUS OF AMENDMENTS

A Response After Office Action Made Final was filed November 20, 2006. No amendments to the application were made in the Response After Office Action Made Final. In response thereto, an Advisory Action was mailed on December 7, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

Some embodiments according to some aspects of the present invention may provide, for example, a wireless communications device as set forth, for example, in claim 1. The wireless communications device may include, for example, a wireless transceiver (e.g., radio 213 of FIG. 2A) and a processor (e.g., Bluetooth baseband core 1709 and FIG. 17). The processor (e.g., Bluetooth baseband core 1709 and FIG. 17) may be coupled to the wireless transceiver (e.g., radio 213 of FIG. 2A). The processor (e.g., Bluetooth baseband core 1709 and FIG. 17) may have a memory (e.g., TX FIFO 1703,

RX FIFO 1705 and FIG. 17 and specification at page 17, lines 25-28) that includes, for example, a plurality of fragments (e.g., fragments 0-127 of FIG. 10 and specification at page 13, lines 3-32) and an array (e.g., linked list 1003 of FIG. 10 and specification at page 13, lines 20-32) configured to control the sequence of memory fragments from which data is read. See, e.g., specification at page 13, lines 20-32.

Some embodiments according to some aspects of the present invention may provide, for example, a processor as set forth in claim 8. The processor (e.g., Bluetooth baseband core 1709 and FIG. 17) may include, for example, a memory (e.g., TX FIFO 1703, RX FIFO 1705 and FIG. 17 and specification at page 17, lines 25-28) having a plurality of fragments (e.g., fragments 0-127 of FIG. 10 and specification at page 13, lines 3-32) and an array (e.g., linked list 1003 of FIG. 10 and specification at page 13, lines 20-32) configured to control the sequence of memory fragments from which data is read. See, e.g., specification at page 13, lines 20-32.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-4 and 8-11 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,426,424 to Dean P. Vanden Heuvel et al. ("Vanden Heuvel").

Whether claims 5-7 and 12-14 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Vanden Heuvel in view of United States Patent No. 5,838,730 to Peter K. Cripps ("Cripps").

ARGUMENT

I. CLAIM 1

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,426,424 to Dean P. Vanden Heuvel et al. ("Vanden Heuvel"). It is respectfully requested that the Board reverse the rejection for at least the reasons as set forth below.

Claim 1 recites "the processor having a memory comprising a plurality of fragments and an array configured to control the sequence of memory fragments from which data is read".

In support of the anticipation rejection, the Office Action Made Final mailed September 19, 2006 ("Office Action Made Final") alleges that

(1) the processor as set forth in claim 1 is processor 106 of FIG. 1 of Vanden Heuvel; and

(2) the memory as set forth in claim 1 is a memory allegedly illustrated in FIG. 5 of Vanden Heuvel.

However, Appellants respectfully draw the attention of the Board to the fact that Vanden Heuvel does not describe either the root array register 501, the control register 503, the memory data are 504 or the free list 505 as part of the processor 106 of FIG. 1 of Vanden Heuvel. Furthermore, Appellants respectfully draw the attention of the Board to the fact that the only memory identified in FIG. 1 of Vanden Heuvel is nonvolatile memory 114, which is also not part of processor 106.

Accordingly, Vanden Heuvel does not describe the processor having a memory that includes a plurality of fragments and an array configured to control the sequence of memory fragments from which data is read as set forth in claim 1.

For at least the above reasons, an anticipation rejection based on Vanden Heuvel cannot be maintained since each and every element as set forth in claim 1 is not described in Vanden Heuvel.

It is therefore respectfully requested that Board reverse the rejection under 35 U.S.C. § 102(b) be reversed with respect to claim 1.

In finding Appellants' arguments unpersuasive, the Examiner states "[t]he examiner would like to point out that the applicant has failed to recognize *memory 115 in fig. 1* of Vanden Heuvel, *which is part of processor 106* [sic] and does include the fragments and array shown in fig. 5 (evidence shown in col. 5, lines 3-18)". Office Action Made Final at page 4 (italics added).

Appellants respectfully draw the attention of the Board to FIG. 1 of Vanden Heuvel: box 115, which is alleged by the Examiner to be the memory that is part of processor 105, is not part of box 105 (i.e., the microcontroller 105 referenced in Vanden Heuvel at col. 5, lines 3-18 cited by the Examiner).

Thus, memory 115 is not part of microcontroller 105 (alleged by the Examiner to be the processor as set forth in claim 1).

Therefore, Vanden Heuvel does not describe "***the processor having a memory*** comprising a plurality of fragments and an array configured to control the sequence of memory fragments from which data is read" as set forth in claim 1.

For at least the above reasons, an anticipation rejection based on Vanden Heuvel cannot be maintained since each and every element as set forth in claim 1 is not described in Vanden Heuvel.

It is therefore respectfully requested that Board reverse the rejection under 35 U.S.C. § 102(b) be reversed with respect to claim 1.

Claim 1 also recites "a wireless transceiver". However, Vanden Heuvel does not describe a wireless transceiver. Instead, Vanden Heuvel describes a receiver. Appellants respectfully draw the attention of the Board to the title of Vanden Heuvel, namely, "Selective Call Receiver with Database Capability". In addition, the Abstract references a "selective call receiver (100)". See Vanden Heuvel at line 1 of Abstract. The selective call receiver 100 is illustrated in FIG. 1 of Vanden Heuvel. The Brief Description of the Drawings describes FIG. 1 as "a block diagram of a selective call receiver that operates in accordance with the preferred embodiment of the present invention". Vanden Heuvel at col. 2, lines 60-62.

Since Vanden Heuvel does not describe a "wireless transceiver" as set forth in claim 1, but instead describes a receiver, namely, a selective call receiver 100, Appellants respectfully submit that the anticipation rejection cannot be maintained since Vanden Heuvel does not describe each and every element as set forth in claim 1.

It is therefore respectfully requested that Board reverse the rejection under 35 U.S.C. § 102(b) be reversed with respect to claim 1.

For at least the above reasons, it is respectfully requested that Board reverse the rejection under 35 U.S.C. § 102(b) be reversed with respect to claim 1.

II. CLAIM 2

Claim 2 depends from claim 1.

Accordingly, at least the reasons set forth above traversing the anticipation rejection with respect to claim 1 are also made with respect to claim 2.

However, the elements as set forth in claim 2, but not set forth in claim 1, are also not anticipated by Vanden Heuvel.

Claim 2 recites "wherein the processor further comprises a second array configured to indicate a status of each of the memory fragments".

In support of the anticipation rejection, the Office Action Made Final alleges that the second array as set forth in claim 2 is control register 503 of FIG. 5 of Vanden Heuvel.

However, Appellants respectfully draw the attention of the Board to the fact that Vanden Heuvel does not describe control register 503 of FIG. 5 as part of the processor 106 of FIG. 1 of Vanden Heuvel. Furthermore, Vanden Heuvel does not describe the control register 503 of FIG. 5 as being configured to indicate a status of each of the memory fragments as set forth in claim 2.

Accordingly, Vanden Heuvel does not describe a processor that includes a second array configured to indicate a status of each of the memory fragments as set forth in claim 2. For at least the above reasons, an anticipation rejection based on Vanden Heuvel cannot be maintained since each and every element as set forth in claim 2 is not described in Vanden Heuvel.

It is therefore respectfully requested that Board reverse the rejection under 35 U.S.C. § 102(b) with respect to claim 2.

III. CLAIM 3

Claim 3 depends from claim 2 which, in turn, depends from claim 1.

Accordingly, at least the reasons set forth above traversing the anticipation rejection with respect to claims 1 and 2 are also made with respect to claim 3.

However, the elements as set forth in claim 3, but not set forth in claims 1 and 2, are also not anticipated by Vanden Heuvel.

Claim 3 recites "wherein the status indicated by the second array for each of the memory fragments comprises a bit to indicate whether its respective memory fragment is empty".

In support of the anticipation rejection, the Office Action Made Final alleges that at least these elements are described in Vanden Heuvel at col. 4, lines 40-46. Appellants respectfully disagree. Col. 4, lines 40-46 of Vanden Heuvel does not describe status indicated by a second array (alleged to be control register 503) that includes a bit to indicate whether its respective memory fragment is empty. In fact, Vanden Heuvel does not describe the previously alleged control register 503 at all. And, even if it did, *for the sake of argument only*, the level of detail as set forth in claim 3 is not described in Vanden Heuvel at col. 4, lines 40-46. Accordingly, the anticipation rejection cannot be maintained since each and every element as set forth in claim 3 is not described in Vanden Heuvel.

It is therefore respectfully requested that the Board reverse the rejection under 35 U.S.C. § 102(b) with respect to claim 3.

IV. CLAIM 4

Claim 4 depends from claim 1.

Accordingly, at least the reasons set forth above traversing the anticipation rejection with respect to claim 1 are also made with respect to claim 4.

However, the elements set forth in claim 4, but not set forth in claim 1, are also not anticipated by Vanden Heuvel.

Claim 4 recites "wherein the processor further comprises a read pointer configured to indicate the memory fragment from which the data is being read".

In support of the anticipation rejection, the Office Action alleges that the processor comprising the read pointer as set forth in claim 4 is read pointer 804 of FIG. 8 of Vanden Heuvel.

However, Appellants respectfully draw the attention of the Board to the fact that Vanden Heuvel does not describe that the read pointers alluded to in FIG. 8 are part of the processor 106 of FIG. 1 of Vanden Heuvel.

Accordingly, Vanden Heuvel does not describe a processor that includes a read pointer configured to indicate a memory fragment from which data is being read as set forth in claim 4. For at least the above reasons, an anticipation rejection based on Vanden Heuvel cannot be maintained since each and every element as set forth in claim 4 is not described in Vanden Heuvel.

It is therefore respectfully requested that the Board reverse the rejection under 35 U.S.C. § 102(b) with respect to claim 4.

V. CLAIM 8

Claim 8 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Vanden Heuvel. It is respectfully requested that the Board reverse the rejection for at least the reasons as set forth below.

Claim 8 recites a processor that comprises a memory having a plurality of fragments and an array configured to control the sequence of memory fragments from which data is read.

In support of the anticipation rejection, the Office Action Made Final alleges that

(1) the processor as set forth in claim 1 is processor 106 of FIG. 1 of Vanden Heuvel; and

(2) the memory as set forth in claim 1 is a memory allegedly illustrated in FIG. 5 of Vanden Heuvel.

However, Appellants respectfully draw the attention of the Board to the fact that Vanden Heuvel does not describe either the root array register 501, the control register 503, the memory data are 504 or the free list 505 as part of the processor 106 of FIG. 1 of

Vanden Heuvel. Furthermore, Appellants respectfully draw the attention of the Board to the fact that the only memory identified in FIG. 1 of Vanden Heuvel is nonvolatile memory 114, which is also not part of processor 106.

Accordingly, Vanden Heuvel does not describe the processor that includes a memory having a plurality of fragments and an array configured to control the sequence of memory fragments from which data is read as set forth in claim 8.

For at least the above reasons, an anticipation rejection based on Vanden Heuvel cannot be maintained since each and every element as set forth in claim 8 is not described in Vanden Heuvel.

It is therefore respectfully requested that Board reverse the rejection under 35 U.S.C. § 102(b) be reversed with respect to claim 8.

VI. CLAIM 9

Claim 9 depends from claim 8.

Accordingly, at least the reasons set forth above traversing the anticipation rejection with respect to claim 8 are also made with respect to claim 9.

However, the elements as set forth in claim 9, but not set forth in claim 8, are also not anticipated by Vanden Heuvel.

Claim 9 recites that the processor of claim 8 comprises a second array configured to indicate a status of each of the memory fragments.

In support of the anticipation rejection, the Office Action Made Final alleges that the second array as set forth in claim 9 is control register 503 of FIG. 5 of Vanden Heuvel.

However, Appellants respectfully draw the attention of the Board to the fact that Vanden Heuvel does not describe control register 503 of FIG. 5 as part of the processor 106 of FIG. 1 of Vanden Heuvel. Furthermore, Vanden Heuvel does not describe the control register 503 of FIG. 5 as being configured to indicate a status of each of the memory fragments as set forth in claim 9.

Accordingly, Vanden Heuvel does not describe a processor that includes a second array configured to indicate a status of each of the memory fragments as set forth in claim

9. For at least the above reasons, an anticipation rejection based on Vanden Heuvel cannot be maintained since each and every element as set forth in claim 9 is not described in Vanden Heuvel.

It is therefore respectfully requested that Board reverse the rejection under 35 U.S.C. § 102(b) with respect to claim 9.

VII. CLAIM 10

Claim 10 depends from claim 9 which, in turn, depends from claim 8.

Accordingly, at least the reasons set forth above traversing the anticipation rejection with respect to claims 8 and 9 are also made with respect to claim 10.

However, the elements as set forth in claim 10, but not set forth in claims 8 and 9, are also not anticipated by Vanden Heuvel.

Claim 10 recites "wherein the status indicated by the second array for each of the memory fragments comprises a bit to indicate whether its respective memory fragment is empty".

In support of the anticipation rejection, the Office Action Made Final alleges that at least these elements are described in Vanden Heuvel at col. 4, lines 40-46. Appellants respectfully disagree. Col. 4, lines 40-46 of Vanden Heuvel does not describe status indicated by a second array (alleged to be control register 503) that includes a bit to indicate whether its respective memory fragment is empty. In fact, Vanden Heuvel does not describe the previously alleged control register 503 at all. And, even if it did, *for the sake of argument only*, the level of detail as set forth in claim 10 is not described in Vanden Heuvel at col. 4, lines 40-46. Accordingly, the anticipation rejection cannot be maintained since each and every element as set forth in claim 10 is not described in Vanden Heuvel.

It is therefore respectfully requested that the Board reverse the rejection under 35 U.S.C. § 102(b) with respect to claim 10.

VIII. CLAIM 11

Claim 11 depends from claim 8.

Accordingly, at least the reasons set forth above traversing the anticipation rejection with respect to claim 8 are also made with respect to claim 11.

However, the elements set forth in claim 11, but not set forth in claim 8, are also not anticipated by Vanden Heuvel.

Claim 11 recites that the processor comprises a read pointer configured to indicate the memory fragment from which the data is being read.

In support of the anticipation rejection, the Office Action alleges that the processor comprising the read pointer as set forth in claim 11 is read pointer 804 of FIG. 8 of Vanden Heuvel.

However, Appellants respectfully draw the attention of the Board to the fact that Vanden Heuvel does not describe that the read pointers alluded to in FIG. 8 are part of the processor 106 of FIG. 1 of Vanden Heuvel.

Accordingly, Vanden Heuvel does not describe a processor that includes a read pointer configured to indicate a memory fragment from which data is being read as set forth in claim 11. For at least the above reasons, an anticipation rejection based on Vanden Heuvel cannot be maintained since each and every element as set forth in claim 11 is not described in Vanden Heuvel.

It is therefore respectfully requested that the Board reverse the rejection under 35 U.S.C. § 102(b) with respect to claim 11.

IX. CLAIMS 5-7

Claims 5-7 stand rejected under 35 U.S.C. § 103(a) as being obvious over Vanden Heuvel in view of United States Patent No. 5,838,730 to Peter K. Cripps ("Cripps"). It is respectfully requested that the Board reverse the rejection for at least the reasons as set forth below.

Claims 5-7 depend directly or indirectly from claim 1.

In view of at least the arguments made above with respect to claim 1, Vanden Heuvel does not teach each and every element as set forth in claim 1 and its rejected

dependent claims (i.e., claims 5-7). Furthermore, Cripps does not make up for the teaching deficiencies of Vanden Heuvel.

For at the above reasons, it is respectfully requested that the rejection under 35 U.S.C. § 103(a) be reversed with respect to claims 5-7.

X. CLAIMS 12-14

Claims 12-14 stand rejected under 35 U.S.C. § 103(a) as being obvious over Vanden Heuvel in view of Cripps. It is respectfully requested that the Board reverse the rejection for at least the reasons as set forth below.

Claims 12-14 depend directly or indirectly from claim 8.

In view of at least the arguments made above with respect to claim 8, Vanden Heuvel does not teach each and every element as set forth in claim 8 and its rejected dependent claims (i.e., claims 12-14). Furthermore, Cripps does not make up for the teaching deficiencies of Vanden Heuvel.

For at the above reasons, it is respectfully requested that the rejection under 35 U.S.C. § 103(a) be reversed with respect to claims 12-14.

XI. CONCLUSION

For the foregoing reasons, it is believed that claims 1-14 are patentable over the alleged prior art of record. Reversal of the Examiner's rejection of claims 1-14 is therefore respectfully requested, thereby placing claims 1-14 in condition for allowance. Accordingly, issuance of a patent on the application is therefore respectfully requested.

The Commissioner is hereby authorized to charge any additional fees, to charge any fee deficiencies or to credit any overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: July 27, 2007

Respectfully submitted,

/Michael T. Cruz/
Michael T. Cruz
Registration No. 44,636

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8000
Facsimile: (312) 775-8100

CLAIMS APPENDIX

The following claims are involved in this appeal:

1. A wireless communications device, comprising:

a wireless transceiver; and

a processor coupled to the wireless transceiver, the processor having a memory comprising a plurality of fragments and an array configured to control the sequence of memory fragments from which data is read.

2. The wireless communications device of claim 1 wherein the processor further comprises a second array configured to indicate a status of each of the memory fragments.

3. The wireless communications device of claim 2 wherein the status indicated by the second array for each of the memory fragments comprises a bit to indicate whether its respective memory fragment is empty.

4. The wireless communications device of claim 1 wherein the processor further comprises a read pointer configured to indicate the memory fragment from which the data is being read.

5. The wireless communications device of claim 1 wherein each of the memory fragments comprises 64 bytes.

6. The wireless communications device of claim 1 wherein the memory fragments comprises 128 memory fragments.

7. The wireless communications device of claim 6 wherein the array comprises a 128 element array.

8. A processor comprising a memory having a plurality of fragments and an array configured to control the sequence of memory fragments from which data is read.

9. The processor of claim 8 further comprising a second array configured to indicate a status of each of the memory fragments.

10. The processor of claim 9 wherein the status indicated by the second array for each of the memory fragments comprises a bit to indicate whether its respective memory fragment is empty.

11. The processor of claim 8 further comprising a read pointer configured to indicate the memory fragment from which the data is being read.

12. The processor of claim 8 wherein each of the memory fragments comprises 64 bytes.

13. The processor of claim 8 wherein the memory fragments comprises 128 memory fragments.

14. The processor of claim 13 wherein the array comprises a 128 element array.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.